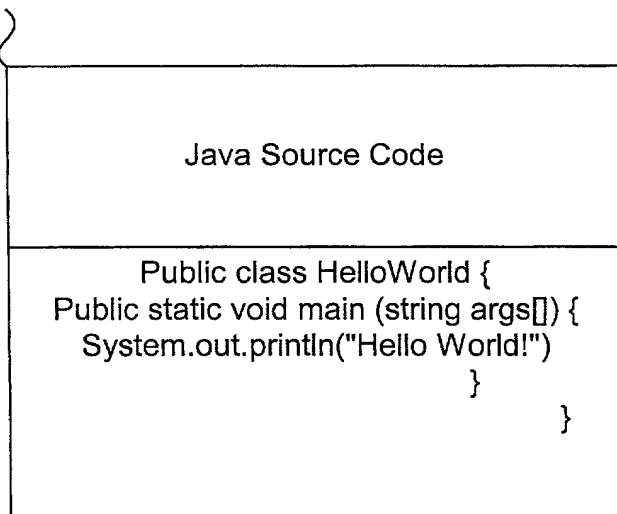
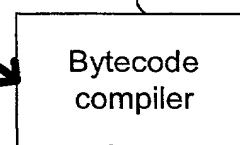


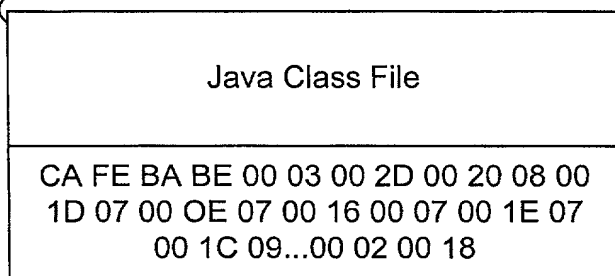
101



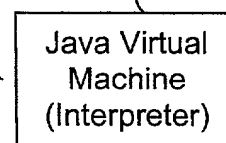
103



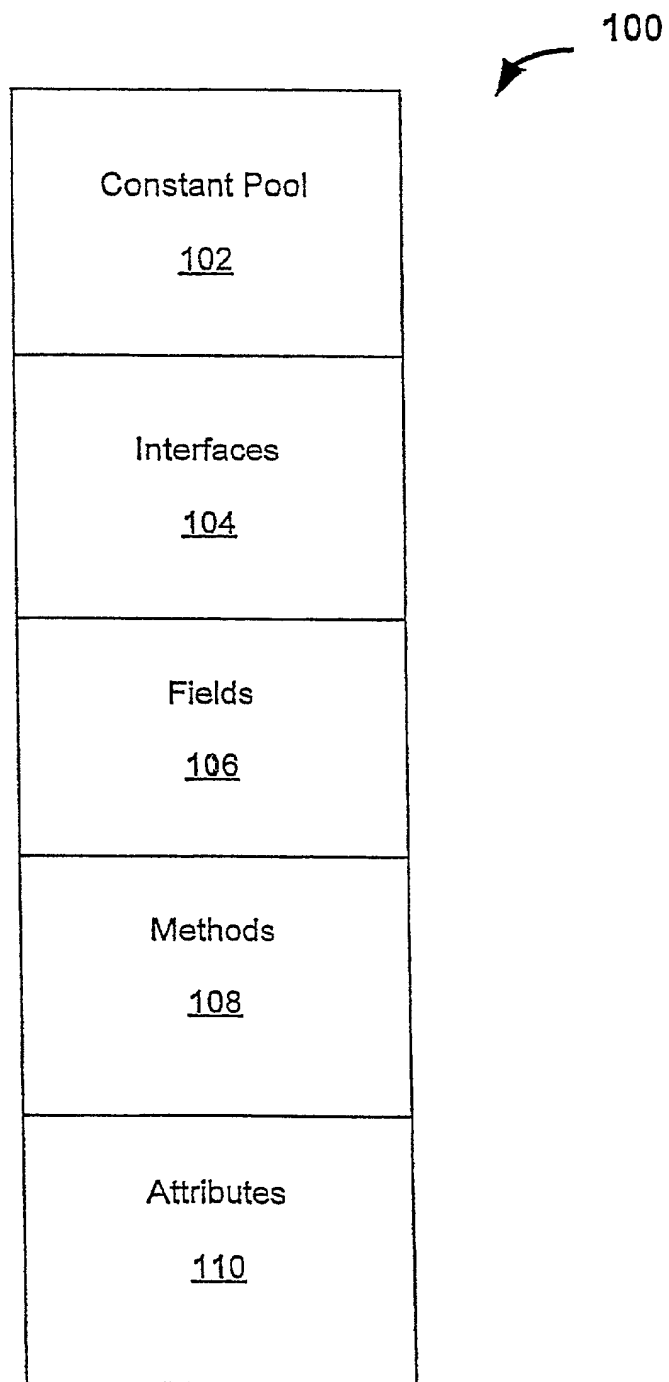
105



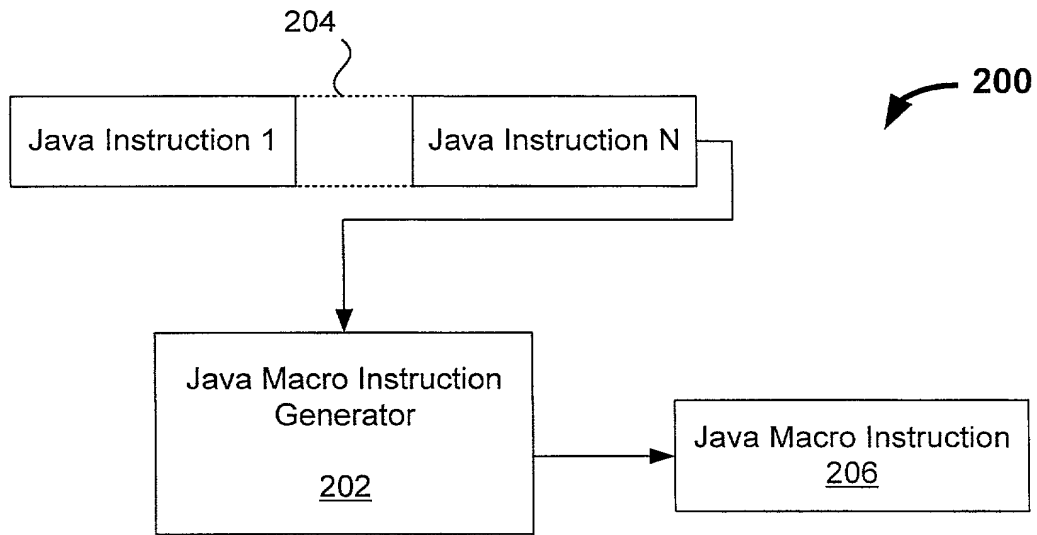
107



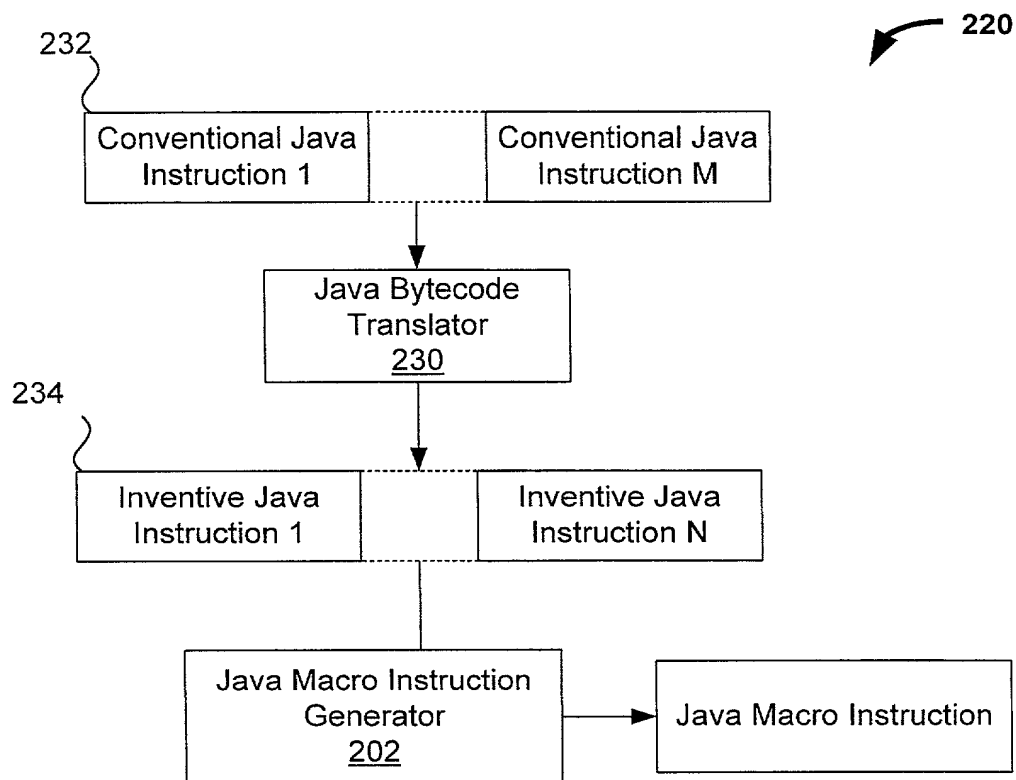
**Fig. 1A**



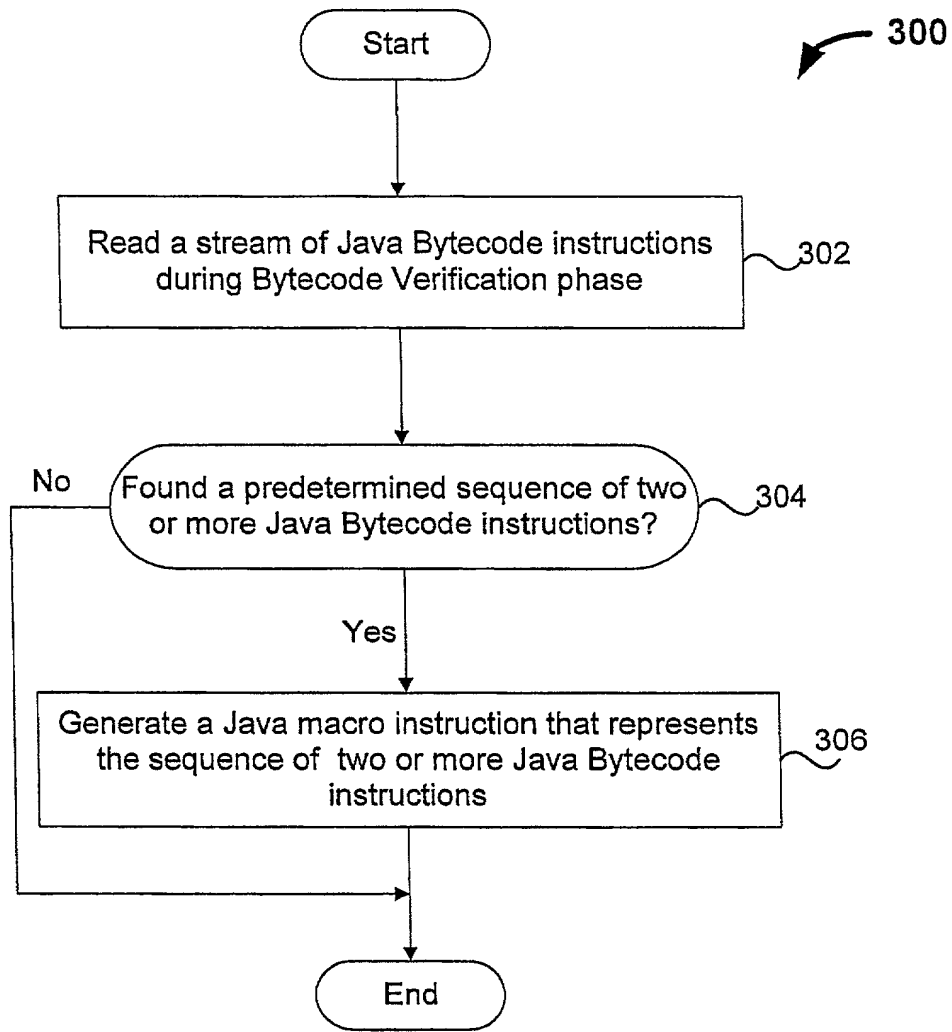
**Fig. 1B**



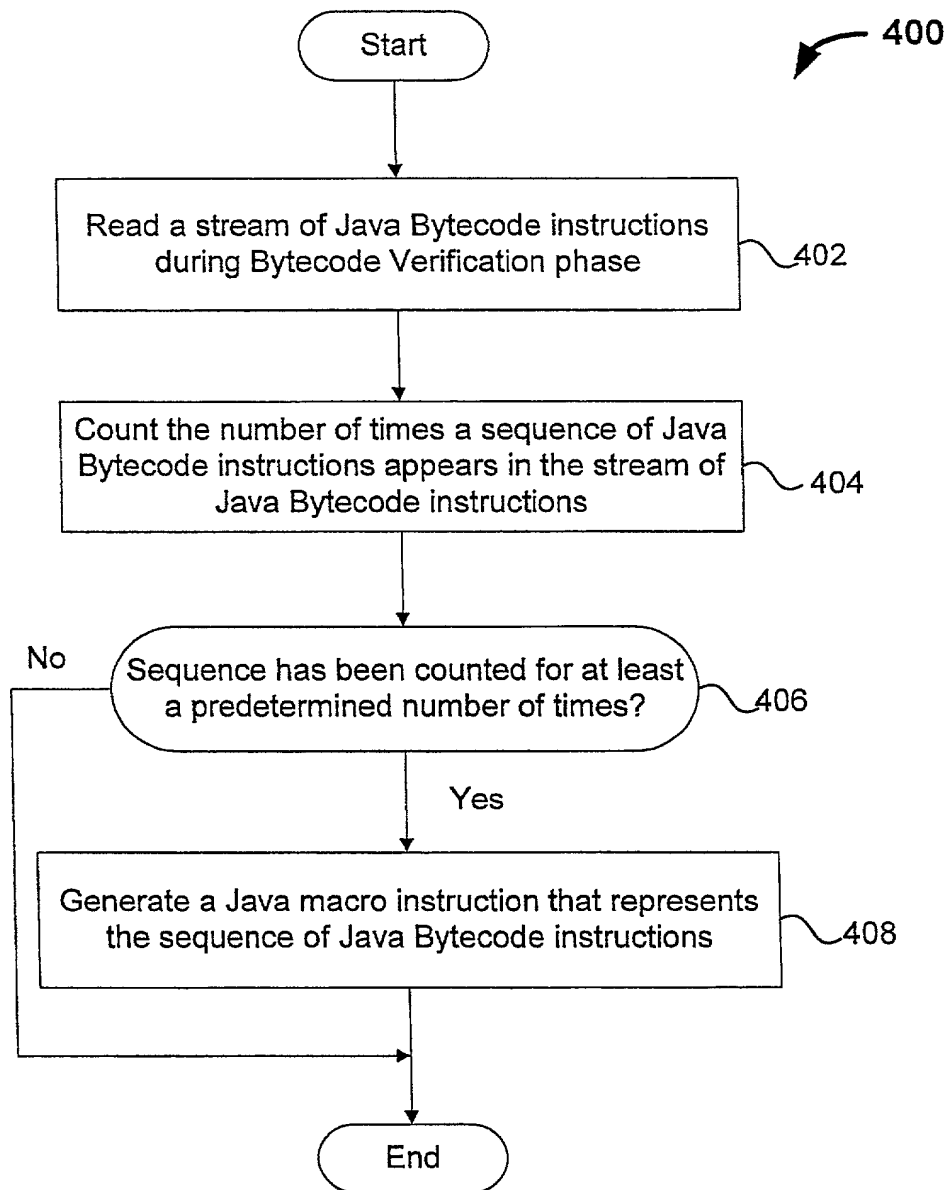
**Fig. 2A**



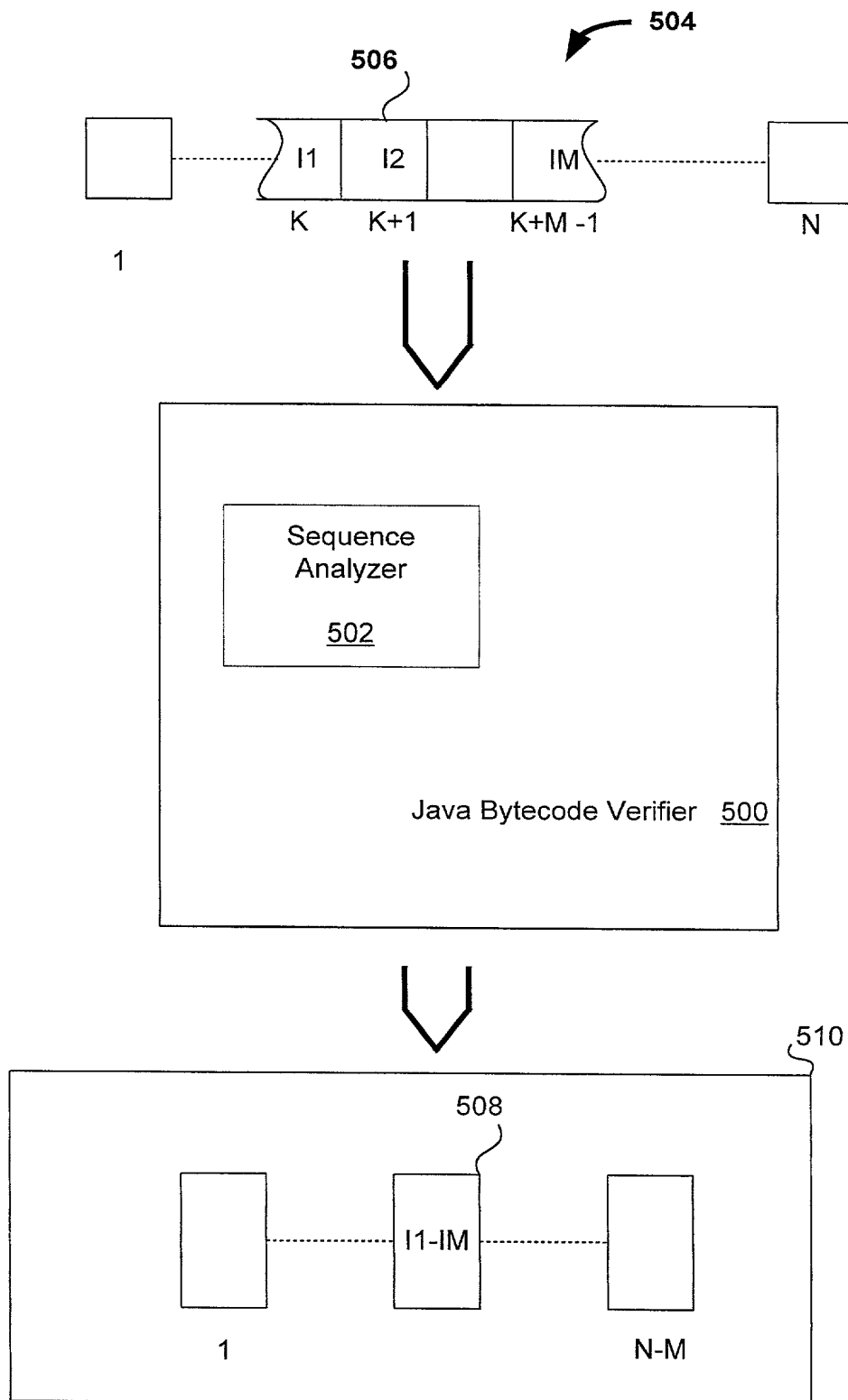
**Fig. 2B**



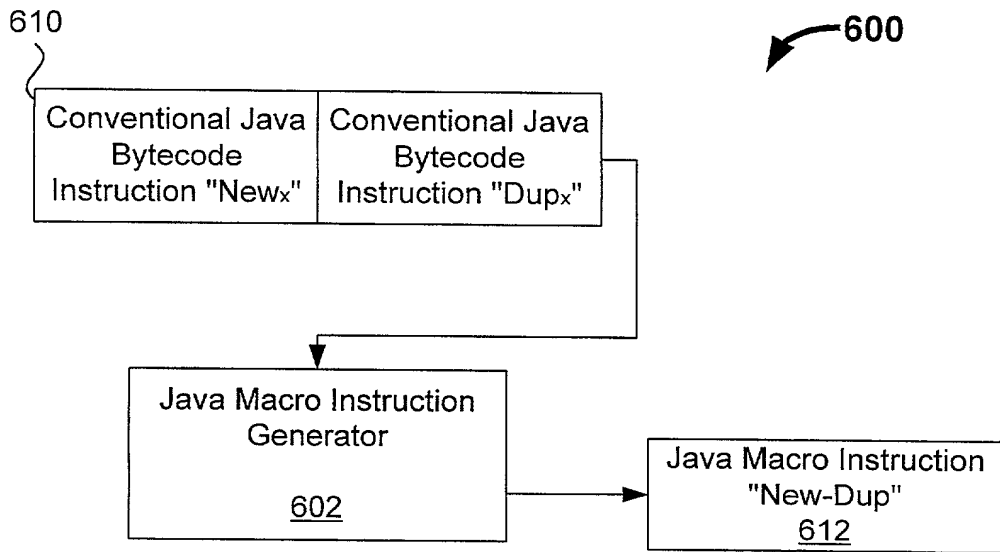
**Fig. 3**



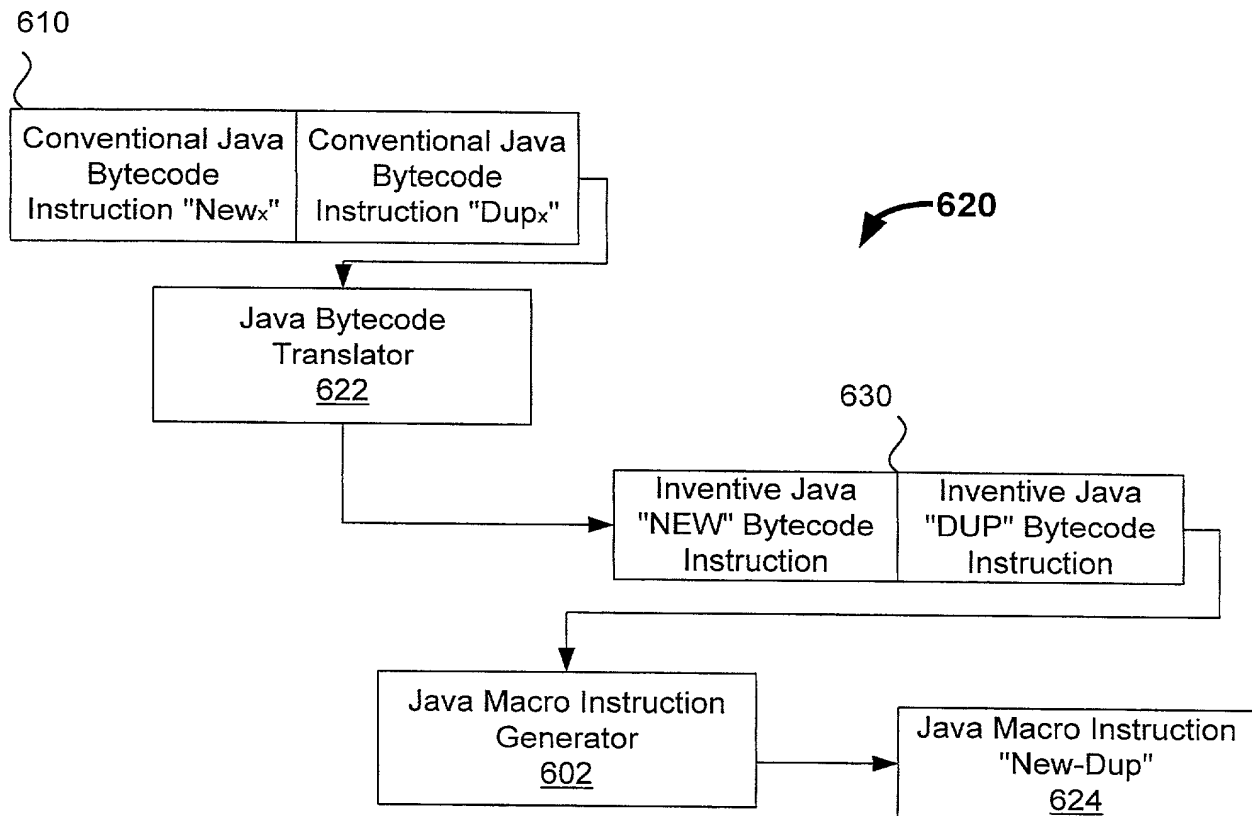
**Fig. 4**



**Fig. 5**

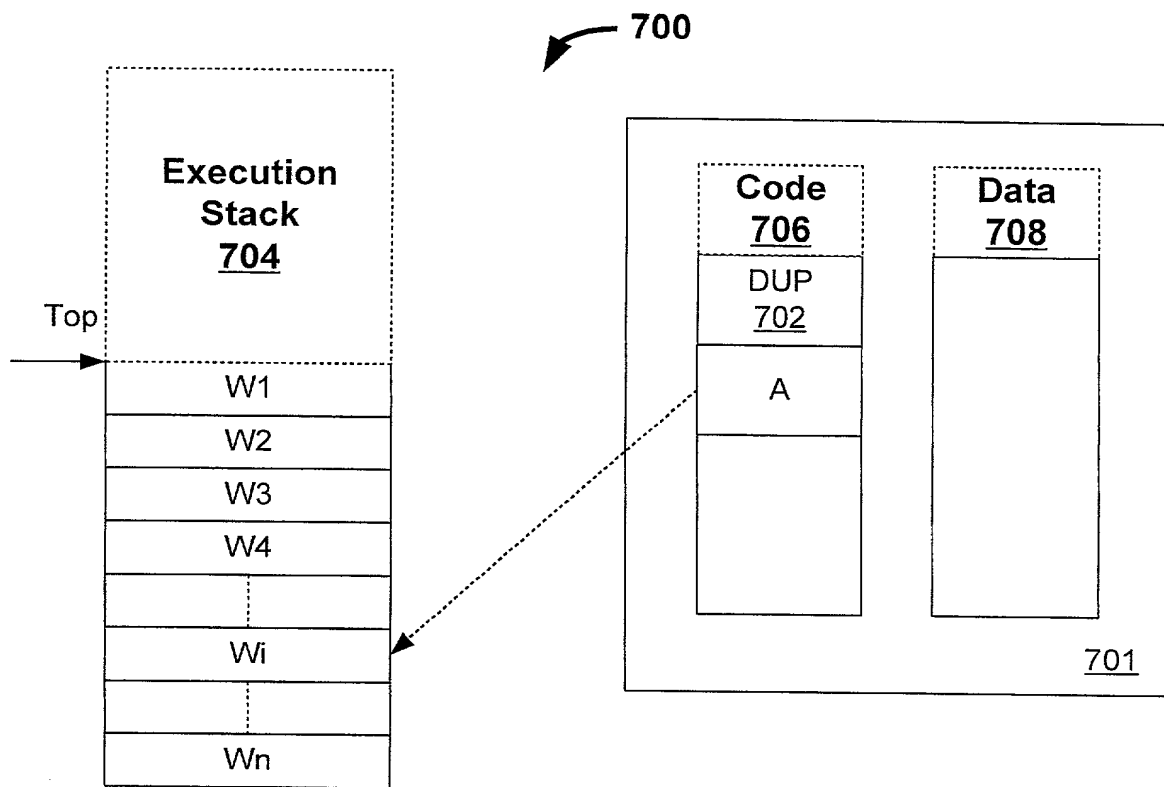


**Fig. 6A**



**Fig. 6B**





**Fig. 7A**

DUP
Dup
Dup_x1
Dup_x2

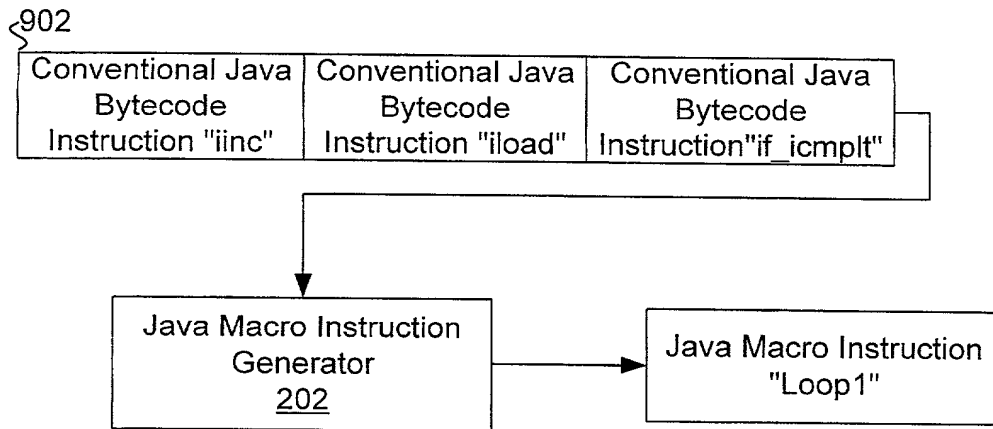
**Fig. 7B**

DUPL
Dup2
Dup2_x1
Dup2_x2

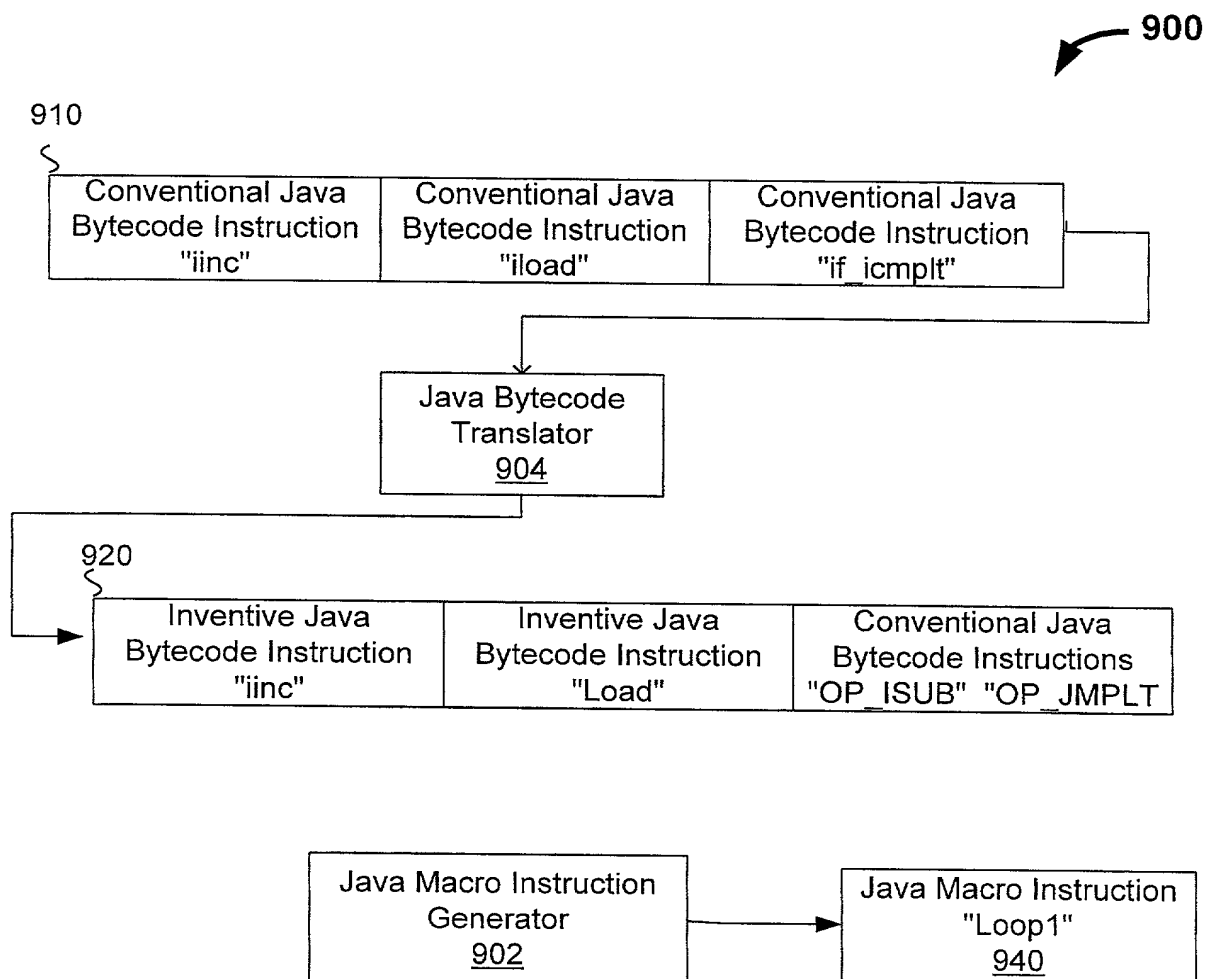
**Fig. 7C**

NEW
New
Newarray
Anewarray
Multianewarray

**Fig. 8**



**Fig. 9A**



**Fig. 9B**

The diagram illustrates a memory layout and an execution stack. At the top, a memory block is divided into two sections: **Code 1002** and **Data 1004**. The **Code 1002** section contains a **Load 1006** instruction. The **Data 1004** section contains an **index i 1008**. A curved arrow labeled **1000** points to the top of the memory block. Below the memory block, the **Execution Stack 1020** is shown. The stack contains several frames, with the top frame labeled **Offset 0** and the bottom frame labeled **Offset i (A)**. Arrows labeled **1022** and **1024** point to the top and bottom of the stack, respectively. A dashed line connects the **index i 1008** in the data section to the **Offset i (A)** in the stack.

**Fig. 10A**

LOAD	
iload	
fload	
aload	
iload_0	
iload_1	
iload_2	
iload_3	
fload_1	
fload_2	
fload_3	
aload_0	
aload_1	
aload_2	
aload_3	

Fig. 10B

LOADL	
lload	
dload	
lload_0	
lload_1	
lload_2	
lload_3	
fload_0	
dload_0	
dload_1	
dload_2	
dload_3	

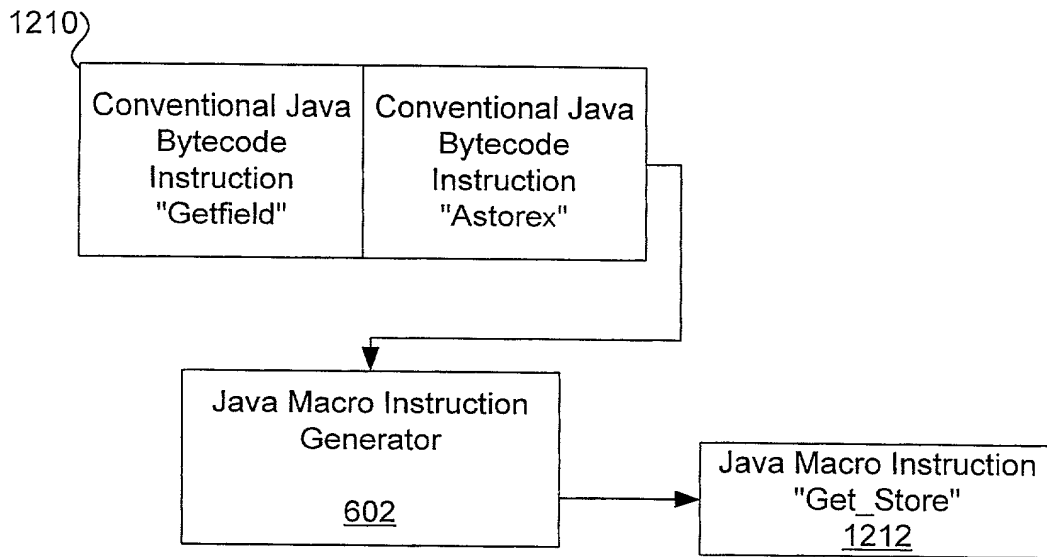
Fig. 10C

lcmp	OP_LSUB, OP_JMPEQ
fcmpl	OP_FSUB, OP_JMPLE
fcmpg	OP_FSUB, OP_JMPGE
dcmpl	OP_DCMP, OP_JMPLE
dcmpg	OP_DCMP, OP_JMPGE

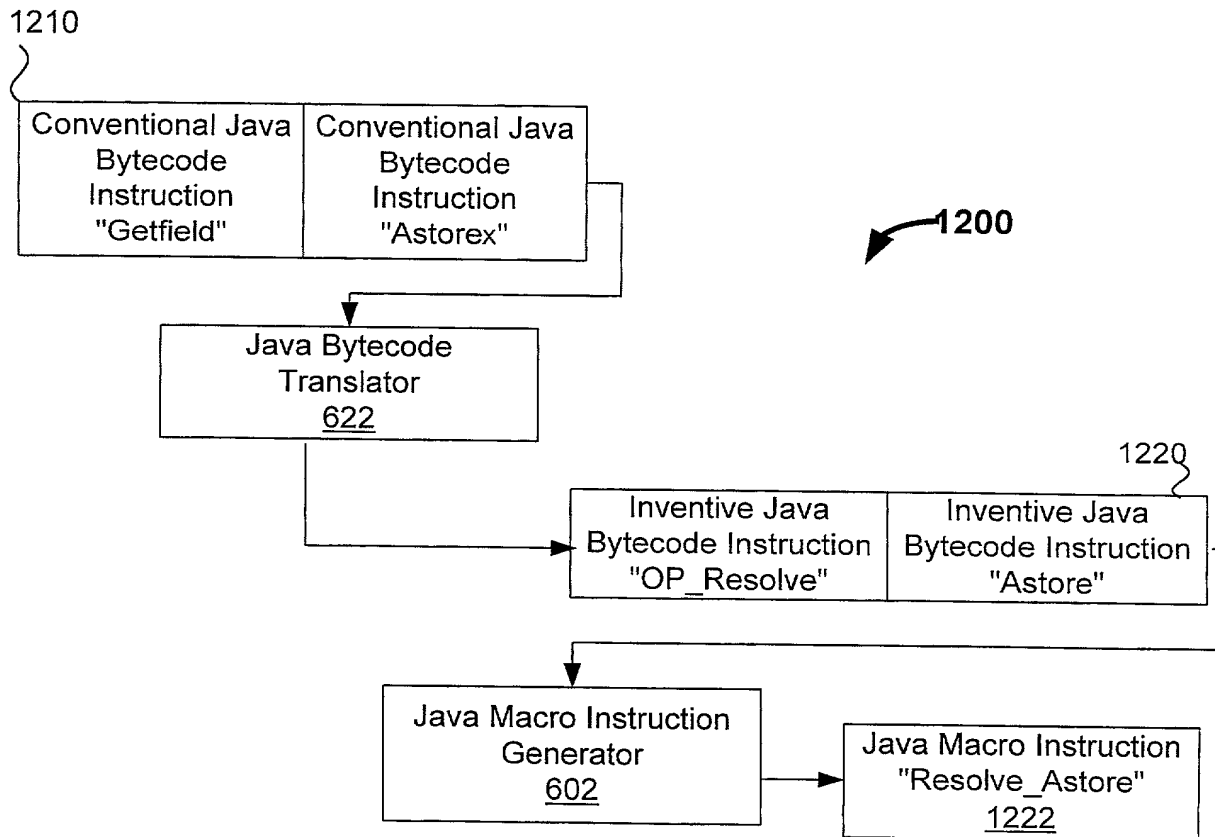
**Fig. 11A**

if_icmpeq	OP_ISUB, OP_JMPEQ
if_icmpne	OP_ISUB, OP_JMPNE
if_icmplt	OP_ISUB, OP_JMPLT
if_icmpge	OP_ISUB, OP_JMPGE
if_icmpgt	OP_ISUB, OP_JMPGT
if_icmple	OP_ISUB, OP_JMPLE
if_acmpeq	OP_ISUB, OP_JMPEQ
if_acmpne	OP_ISUB, OP_JMPNE

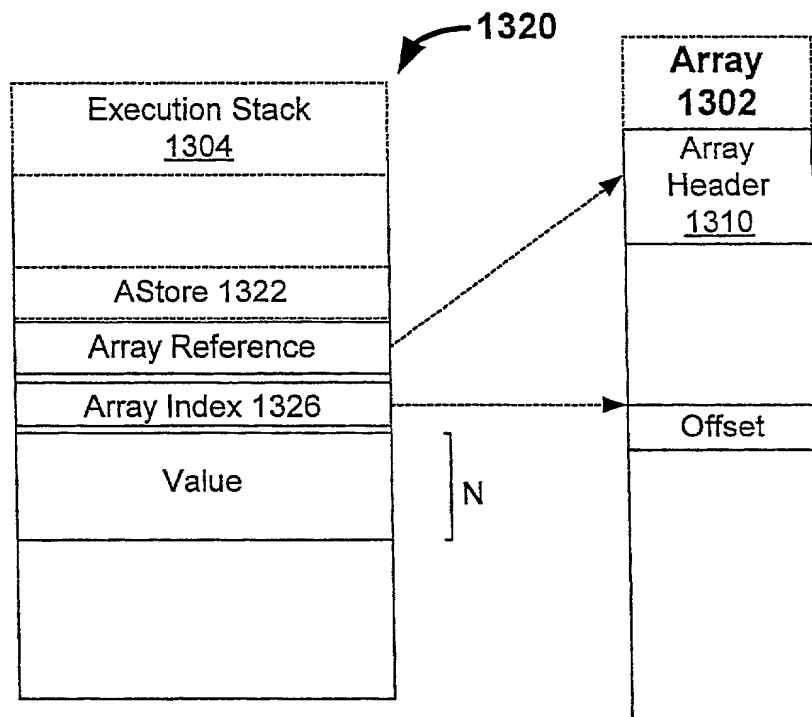
**Fig. 11B**



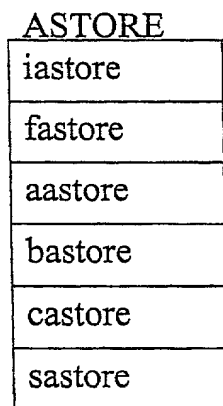
**Fig. 12A**



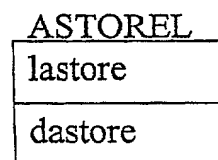
**Fig. 12B**



**Fig. 13A**



**Fig. 13B**



**Fig. 13C**